Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An advanced process control (APC) method for ~~an oxide, metal, or barrier~~ a target layer polish process in a polish tool that minimizes within wafer and wafer to wafer sheet resistance (Rs) variations in a plurality of wafers having a metal layer formed on a barrier layer within an opening in a dielectric layer, said metal layer has a thickness, width, and cross-sectional area, comprising:

[[(a)]] providing a plurality of wafers each having a metal layer that has been formed on a barrier layer within an opening in a dielectric layer by a sequence of processing steps; ~~said processing steps include at least one patterning step, CVD step, etch step, and metal deposition step;~~

[[(b)]] determining a relationship between the cross-sectional area of said metal layer and Rs;

[[(c)]] determining a total Rs (Rs_{TOTAL}) for the metal layer on each of said plurality of wafers before said ~~oxide, metal, or barrier~~ target layer polish process;

[[(d)]] determining ~~an oxide, metal, or barrier~~ a target layer polish thickness target for said metal layer on each of said plurality of wafers; and

[[(e)]] calculating ~~an oxide, metal, or barrier~~ a target layer polish time for each of said plurality of wafers in the ~~oxide, metal, or barrier~~ target layer polish process.

2. (Currently Amended) The method of claim 1 wherein said metal layer is comprised of copper and the barrier layer is comprised of TaN and said ~~oxide, metal, or barrier~~ target layer polish process is performed in a CMP tool that polishes one or more of said copper layer, TaN barrier layer, and dielectric layer simultaneously.

3. (Currently Amended) The method of claim 1 wherein the relationship between the cross-sectional area of said metal layer and Rs is determined by plotting ~~(1/cross-sectional~~

~~area)~~ 1/cross-sectional area vs. Rs results for a plurality of wafers and line fitting the data.

4. (Original) The method of claim 1 wherein the total Rs is determined from the equation:

$$Rs_{TOTAL} = Rs_{PHOTO} + Rs_{CVD} + Rs_{ECP} + Rs_{ETCHING}$$

where Rs_{PHOTO}, Rs_{CVD}, Rs_{ECP}, and $Rs_{ETCHING}$ are terms that represent contributions from a patterning (photo) step, a CVD step, a metal deposition (ECP) step, and an etching step, respectively, to a variation in the width and thickness of said metal layer.

5. (Currently Amended) The method of claim 1 wherein said ~~oxide, metal, or barrier~~ target layer polish thickness target for said metal layer is determined from the relationship ~~in step (b)~~ between the cross-sectional area of said metal layer and Rs, the Rs_{TOTAL}, and the desired Rs value (Rs target value) for said metal layer in each of the plurality of wafers.

6. (Currently Amended) The method of claim 1 wherein the ~~oxide, metal, or barrier~~ target layer polish time is determined by using the equation:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha$$

where PT_t is the polish time for a particular wafer, Rs_T is the Rs target value provided for said metal layer, α is the polish rate in said ~~oxide, metal, or barrier~~ target layer polish process, and Rs_{TOTAL} is the value from the second determining step [[(c)]].

7. (Currently Amended) The method of claim 6 further comprised of modifying the target layer polish time ~~in step (e)~~ based on a post ~~oxide, metal, or barrier~~ target layer polish measurement data by including a disturbance factor (d_K) wherein the modified equation is the following:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha + d_K$$

where $d_K = (1 - \lambda)d_{K-1} + \lambda\,(Rs_T - Rs_{n,\,TOTAL} - \alpha\,PT_{K-1})$ in which d_{K-1} and PT_{K-1} indicate a

disturbance factor and the target ~~oxide, metal, or barrier~~ layer polish time, respectively, for the (n-1)th wafer in the plurality of wafers, $Rs_{n,\ TOTAL}$ is Rs_{TOTAL} for the nth wafer in a plurality of wafers, and λ is a numerical value between 0 and 1.

8. (Currently Amended) The method of claim 7 wherein d_{K-1} is equal to 0 for the first wafer in the plurality of wafers to be ~~oxide, metal, or barrier layer~~ polished in the target layer polish process.

9. (Currently Amended) The method of claim 7 wherein said a post ~~oxide, metal, or barrier~~ target layer polish measurement data includes the polish rate of said metal layer in said ~~oxide, metal, or barrier~~ target layer polish step on at least one wafer that has been processed in the process tool.

10. (Original) The method of claim 7 wherein any filter algorithm may be used to update said d_{K-1}.

11. (Currently Amended) The method of claim 1 wherein said ~~steps (b) — (e)~~ first determining, second determining, third determining, and calculating steps are performed by a computer that is part of an advanced process control (APC) system which includes an APC controller that receives input from the computer and sends commands to one or more polish tools via a tool application program (TAP) and tool control system (TCS).

12. (Currently Amended) The method of claim 11 wherein the computer contains a feed forward (FF) model and a feed backward (FB) model wherein the FF model receives measurement data related to said sequence of processing steps and is used to perform the second determining, the third determining, and the calculating steps ~~(c) — (e)~~ and wherein the FB model receives post ~~oxide, metal, or barrier~~ target layer polish measurement data and is also used for the calculating step [[(e)]].

13. (Currently Amended) An APC method for an oxide (Cu, or TaN) polish step in a CMP tool that minimizes within wafer and wafer to wafer sheet resistance (Rs) variations in a plurality of wafers having a copper layer, said copper layer has a thickness, width, and cross-sectional area and is formed on a TaN layer in an opening within a dielectric layer, comprising:

[[(a)]] providing a plurality of wafers each having a copper layer that has been formed on a TaN layer in an opening within a dielectric layer by a sequence of processing steps;~~-said processing steps include at least one patterning step, CVD step, etch step, and copper deposition step;~~

[[(b)]] determining a relationship between the cross-sectional area of said copper layer and Rs;

[[(c)]] determining a total Rs for the copper layer on each of said plurality of wafers before said oxide (Cu, or TaN) polish process;

[[(d)]] determining an oxide (Cu, or TaN) polish thickness target for said copper layer on each of said plurality of wafers; and

[[(e)]] calculating an oxide (Cu, or TaN) polish time for each of said plurality of wafers in the oxide (Cu, or TaN) polish process.

14. (Original) The method of claim 13 wherein said oxide (Cu, or TaN) polish process reduces the thickness of one or more of said copper layer, TaN layer, and dielectric layer.

15. (Currently Amended) The method of claim 13 wherein said opening is <u>at least one of</u> a trench [[or]] <u>and</u> a trench formed above a via.

16. (Currently Amended) The method of claim 13 wherein the relationship between the cross-sectional area of said copper layer and Rs is determined by plotting ~~(1/cross-sectional area)~~ <u>1/cross-sectional area</u> vs. Rs results for a plurality of wafers and line fitting the data.

17. (Original) The method of claim 13 wherein the total Rs is determined from the equation:

$$Rs_{TOTAL} = Rs_{PHOTO} + Rs_{CVD} + Rs_{ECP} + Rs_{ETCHING}$$

where Rs_{PHOTO}, Rs_{CVD}, Rs_{ECP}, and $Rs_{ETCHING}$ are terms that represent contributions from a patterning (photo) step, a CVD step, a copper deposition (ECP) step, and an etching step, respectively, to a variation in the width and thickness of said copper layer.

18. (Currently Amended) The method of claim 13 wherein said oxide (Cu, or TaN) polish thickness target for said copper layer is determined from the relationship ~~in step (b)~~ <u>between the cross-sectional area of said metal layer and Rs</u>, the Rs_{TOTAL}, and the desired Rs value (Rs target value) for said copper layer in each of the plurality of wafers.

19. (Currently Amended) The method of claim 13 wherein the oxide (Cu, or TaN) polish time is determined by using the equation:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha$$

where PT_t is the polish time for a particular wafer, Rs_T is the Rs target value provided for said copper layer, α is the polish rate in said oxide (Cu, or TaN) polish process, and Rs_{TOTAL} is the value from <u>the second determining</u> step [[(c)]].

20. (Currently Amended) The method of claim 19 further comprised of modifying the polish time in <u>the calculating</u> step (e) based on post oxide (Cu, or TaN) polish measurement data by including a disturbance factor (d_K) wherein the modified equation is the following:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha + d_K$$

where $d_K = (1 - \lambda)d_{K-1} + \lambda\,(Rs_T - Rs_{n,\,TOTAL} - \alpha\, PT_{K-1})$ in which d_{K-1} and PT_{K-1} indicate a disturbance factor and oxide (Cu, or TaN) polish time, respectively, for the (n-1)th wafer in the plurality of wafer, $Rs_{n,TOTAL}$ is Rs_{TOTAL} for the nth wafer in a said plurality of wafers, and λ is a numerical value between 0 and 1.

21. (Original) The method of claim 20 wherein d_{K-1} is equal to 0 for the first wafer in the plurality of wafers to be polished in the oxide (Cu, or TaN) polish process.

22. (Original) The method of claim 20 wherein said post oxide (Cu, or TaN) polish measurement data include the polish rate of said copper layer in said oxide (Cu, or TaN) polish step on at least one wafer that has been processed in the process tool.

23. (Original) The method of claim 20 wherein any filter algorithm may be used to update said d_{K-1}.

24. (Currently Amended) The method of claim 13 wherein said ~~steps (b) — (e)~~ first determining, second determining, third determining and calculating steps are performed by a computer that is part of an advanced process control (APC) system which includes an APC controller that receives input from the computer and sends commands to one or more polish tools via a tool application program (TAP) and tool control system (TCS).

25. (Currently Amended) The method of claim 24 wherein the computer contains a feed forward (FF) model and a feed backward (FB) model wherein the FF model receives measurement data related to said sequence of processing steps and is used to perform the second determining, the third determining, and the calculating steps ~~(c) — (e)~~ and wherein the FB model receives post oxide (Cu, or TaN) polish measurement data and is also used for the calculating step [[(e)]].

26. (Original) The method of claim 24 wherein said APC controller is linked to more than one CMP process tool and to more than one computer that provides data input.

27-40. (Cancelled).

41. (New) The method of claim 1, wherein the target layer is at least one of an oxide, a metal, and a barrier layer.

42. (New) The method of claim 1, wherein the processing steps include at least one patterning step, CVD step, etch step, and metal deposition step.

43. (New) The method of claim 13, wherein said processing steps include at least one patterning step, CVD step, etch step, and copper deposition step.